PLC2 DESIGN

Did you know we are a expert in

Automated Test Enviroments

Creating Automatic Validations Systems in Simulation and in real Hardware

Every time when a new product is designed, time should be spent to think about the validation of the whole system. It is important to know at an early phase of the project. how to test the design when it is developed and ready for testing.
With the use of VHDL and OSVVM, a complex simulation can be done. The whole simulation process can be automated. Every time something in the FPGA design changes, every functionality is tested automatically when the simulation is started.
In addition to simulation, the developed design can be tested in hardware in the real world. A HiL-Simulation (Hardware in the Loop) can be done. In that case, the developed system is tested automatically in hardware, by connecting the inputs and outputs to a verification hardware. This can be done to verify the functionality of a developed system and/or to test devices which are built in serial production.
We create testbenches and HiL-Simulation systems to verify your embedded systems.