



Workshop ZYNQ UltraScale+ MPSoC System Architecture

The 2-day workshop will focus on the system architecture of the XILINX Zynq UltraScale+ MPSoC devices.

Starting with the general overview of this technology the next topics showing the details of the hardware architecture and use cases of the Processing System (PS).

Especially the power management with the Platform Management Unit (PMU) in the PS is a feature of the ZYNQ MPSoC architecture which enable customizable watchdogs and dynamic power optimization.

With several sharing memory resources the user can configure its access in PS and PL via AXI ports with supported hardware coherency management.

As next system-specific features such as System Protection and clock and reset structures discussed.

The DDRAM Controller enables multiple port arbitration, prioritization, flow control, and class traffics like Video

stream storage.

The boot and configuration process of the Zynq UltraScale+ MPSoC components are discussed in detail.

During the individual chapters, various exercises, which are carried out independently by the participants, will be provided.

Applicable technologies

XILINX ZYNQ UltraScale+ MPSoC & RFSoc

Requirements

Good understanding of digital embedded systems
Basic knowledge of the programming language C

Duration and Costs:

Duration: 2 days

Cost: € 1.500 net per person, including detailed training material, drinks in the breaks and lunch

Agenda

Day 1:

- ZYNQ UltraScale+ MPSoC Overview
- ZYNQ UltraScale+ MPSoC Application Processing Unit
- ZYNQ UltraScale+ MPSoC Real-Time Processing Unit
- ZYNQ UltraScale+ MPSoC HW-SW Virtualization
- ZYNQ UltraScale+ MPSoC Power Management
- ZYNQ UltraScale+ MPSoC System Coherency
- ZYNQ UltraScale+ MPSoC System Protection

Day 2:

- ZYNQ UltraScale+ MPSoC Clocks and Resets
- ZYNQ UltraScale+ MPSoC DDR and QoS
- ZYNQ UltraScale+ MPSoC Boot and Configuration
- ZYNQ UltraScale+ MPSoC Ecosystem Support

Accompanying exercises allow a practice-oriented training