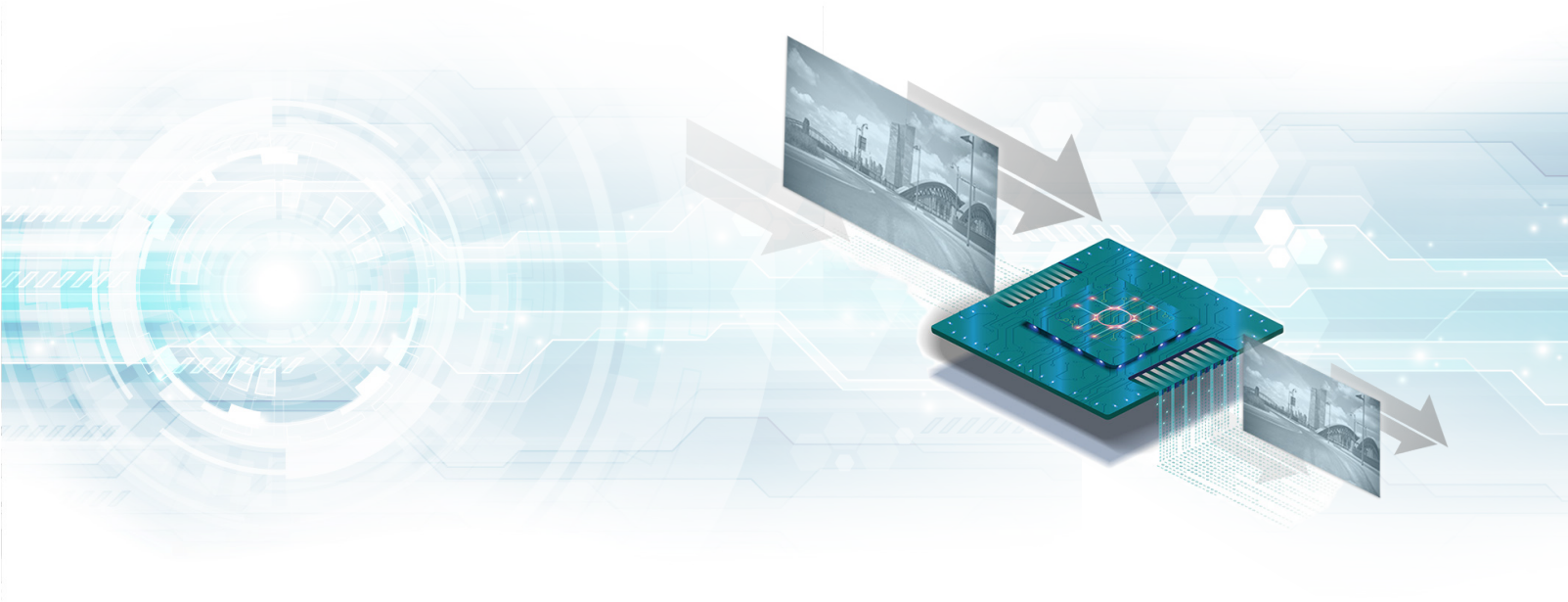
L5 (De-)Compression IP

Lossless - Low Latency - Low Power - Lightweight

The PLC2 Lossless, Low Latency, Low Power & Lightweight (L5) Compression IP is an image Compression IP for FPGAs. It is packaged with Xilinx AXI4-Streaming interfaces to be seamlessly attached to existing image processing applications.
With the PLC2 L5 Compression you can achieve state of the art sub-frame latency combined with low power consumption, a lightweight implementation in terms of resource consumption and lossless Decompression for a wide range of applications on the edge and in the cloud, without having to invest in new and powerful hardware. The target use cases for our L5 (De-) Compression IP are camera based applications in the automotive industry (including heavy duty trucks), railway applications, robots, drones, etc. With a lossless data reduction of up to 60 % costly storage space is saved and room will be created for e.g. the future usage of higher resolution sensors and new types of applications.



Key Facts*

Savings	~ 30 % - 70 %
Power estimation	< 0.05 W
Resource consumption	< 5000 CLBs (LUT & Reg together) & 18 DSPs
Frame Latency	< 1 frame
Features	
Formats	Bayer Pattern (RCCG, RGGB, RCCC, etc.) Gray, YUV422 Stereo-disparity
Bit depths	Up to 16 bit
Resolutions	Configurable

**** Resolution: 2.4 MP, 16 bpp / processing at 100 MHz with 2 pixel per beat / on own data-set***

PLC2 PRODUCTS

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