XILINX XPERTS XILINX Program for Engineering Resources from Third Parties

PLC2 PROGRAMMABLE LOGIC COMPETENCE CENTER

XILINX VERSAL™

Workshop VERSAL ACAP – Connectivity

New

The XILINX VERSAL Adaptive Compute Acceleration Platform (ACAP) allows very fast interfaces to external components based on significantly improved silicon structures as well as new IP Core configuration wizards. Realization challenges are shifting from chip level to board level with the new VERSAL platform. Extreme accuracy in PCB design is mandatory to achieve high-speed data rates.

The 3-day Workshop"VERSAL ACAP – Connectivity" has been developed for hardware designers, system architects and layout designers who want to successfully implement high-speed interfaces in their systems.

This workshop starts with an introduction to VERSAL ACAP including discussion on the IO and clocking resources. Signal interfacing is discussed in detail before discussing in depth designing for DDR4 and serial transceivers. Special focus is on the Network-on-Chip (NoC) as new high-performance connectivity structure inside ACAP devices.

All design steps are described: IP configuration, functional simulation, and implementation. Designs will be verified on real hardware once VERSAL boards are available. Additional focus is put on the physical layer – PCB design and signal integrity. Practical design and verification examples are discussed. Students learn how to apply design rules to the PCB design.

Methodical tips and tricks are provided throughout the training. Exercises in VERSAL ACAP devices intensify students' acquired knowledge.

Applicable technologies

VERSAL ACAP

Requirements

Basic knowledge on VHDL and FPGA implementation

Duration and Costs:

Duration: 3 days

Cost: € 2.100 net per person, including detailed training material, drinks in the breaks and lunch.

Agenda

Introduction

Architecture Overview and Clocking

- VERSAL ACAP architecture
- IO architecture and resources
- Clock architecture and resources

Signal Interfacing

- IO standards, termination
- Banking rules
- PCB rules and pin definition

Platform management controller

- Network-on-Chip (NoC)
- Introduction and NoC concept
- NoC flow methodology
- NoC performance simulation
- Application examples

Memory Interfacing

- DDR memory controller architecture and functionality
- MC configuration
- Design rules
- Realization of other memory interfaces
- Design practice

Transceivers

- Transceiver overview
- PCS blocks and usage options
- PMA layer options
- Simulation and implementation
- PCB requirements and design guidelines
- Signal Integrity simulation options

Powering

- Power estimation and tools
- Power distribution, filtering and decoupling
- Powering realization options

Labs

- Various labs deepen the knowledge and allowing practice-oriented training