XILINX XPERTS XILINX Program for Engineering Resources from Third Parties

PLC2 PROGRAMMABLE LOGIC COMPETENCE CENTER

Workshop Compact FPGA Design Techniques

For the successful implementation of the digital circuits in the FPGA, the strong knowledge of the digital circuit's basics is mandatory. The HDL based developing method simplifies the developing cycle but for that developer must have the good knowledge of digital circuit design. Although most of developer basically knows the digital components like combinational and sequential and there usage but some of their knowledge got lost due to time or some developer have not learned e.g. that's the fact when software programmer has to develop FPGA'S without special previous knowledge.

The three days workshop "Compact FPGA Design Techniques" gives the FPGA developers a solid and detailed knowledge in the area of digital circuit techniques.

Furthermore the arithmetic operations and their implementation will be discussed in detail after this we will discuss examples of combination circuits like encoder, decoder, and multiplexer. Moreover the RTL design techniques will be presented with the RTL components like counters, frequency generators etc. The errors which can be occur during clock generation and clock distribution will be discussed in brief. In the next section we will see the implementation of digital circuits with the memory devices like RAM'S, ROM'S etc. The final section consists of brief introduction to the XILINX FPGA'S as target device for implementation of digital circuits.

Applicable technologies

All kind of FPGA technologies

Requirements

None

Duration and Cost

Duration: 3 days

Cost: € 2.100, – net per person, including detailed training material, drinks in the breaks and lunch.

Agenda

Introduction to the FPGA Architecture (XILINX 7-Series)

- Combinatorial Resources
- Sequential Resources
- Embedded Resources
- Clock Resources & MMCM
- RAMs and FIFOs
- Input / Output Resources

Design Techniques

- Synchronous vs. Asynchronous
- Synchronous Design Techniques
  - Clock Structures
  - Reset Structures
  - Pipelining
- Designing with RAMs and FIFOs
- Designing Interfaces
  - SDR / DDR Interfaces
  - Asynchronous Interfaces
  - Low Speed Interfaces
- Rules and Best Practice

Clock Domain Crossing (CDC)

- Sampling and Capturing Data in Multiple Clock Domains
- Synchronization Circuits
- CDC Analysis

Labs

- Design of an UART
- Low Speed DAC Interface using SPI