XILINX XPERTS XILINX Program for Engineering Resources from Third Parties

PLC2 PROGRAMMABLE LOGIC COMPETENCE CENTER

VIVADO

Workshop
Advanced VIVADO HLS

One thing coming increasingly to the fore is the acceleration of computation intensive applications such as used in e.g. image processing or specific DSP algorithms.

Vivado High Level Synthesis (HLS) allows to quickly and efficiently port those algorithms to hardware. Usage of 'C' based high level languages like 'C', 'C++' or 'SystemC' automates the implementation and optimisation of FPGA designs by converting the 'C' based code to HDL (VHDL or Verilog).

This allows various scenarios when used in combination with ZYNQ-7000 SoC technology: For Example 'C++' algorithms can be run either on the ZYNQ as software or they can be implemented in the programmable logic as hardware. Moreover, targeting hardware, the algorithms can be optimised for speed, latency or resource usage. The focus of this workshop is put on using the HLS environment to create hardware accelerators for computation intensive applications. Working on exercises, the attendee creates 'C'/'C++' programs that are run as software on a MicroBlaze/ ZYNQ processor in a first step. In a second step, the code is converted to RTL code and gets implemented.

This workshop's target audience are attendees with a first experience using Vivado HLS as well as basic knowledge of 'C'/'C++' and VHDL. Furthermore, the attendee should be familiar with the ZYNQ device or the MicroBlaze processor and the associated development tools.

Applicable technologies

XILINX 7-Series and UltraScale FPGAs

Requirements

Basic knowledge of Vivado HLS

Basic knowledge of 'C'/'C++'

Experience in Using ZYNQ-SoC and/or MicroBlaze of advantage

Duration and Costs:

Duration: 3 days

Cost: € 2.100,- net per person, including detailed training material, drinks in the breaks and lunch

Agenda

Review Vivado HLS
- Create the optimum Architecture
- Control and Data Path Extraction
- Function and Hierarchy
- Top Level I/O and Interfaces

Review Throughput & Latency
- Adding Directives
- Improving Throughput and Latency

Processor based Hardware Design
- IP Integrator
- Adding AXI based Peripherals
- Custom Peripheral Design

XILINX SDK
- Software Development
- Writing Device Driver
- Performance Analysis

ZYNQ Development Flow to Accelerated C
- Accelerator: An Overview
- Understand Interconnect Performance
- Integrate Accelerated C Function

Accelerating OpenCV Applications
- ZYNQ based OpenCV Application
- OpenCV design flow
- API and HLS Directives

DSP and Video C Library Overview
- Vivado HLS Libraries
- XILINX Linear Algebra HLS Library
- Open CL
- Ecosystem Libraries

Labs
- **Lab:** Designs Analysis and Optimization
- **Lab:** Acceleration for mathematical applications
- **Lab:** Acceleration Graphic applications
- **Lab:** Acceleration of DSP applications