NEW

Compact VITIS

Accelerate Applications as FPGA Kernels

Sequential processing or data path speed is a bottleneck in many high-end systems based on CPUs. Whereas FPGAs provide massive parallel data processing along with optimized data path. A system with CPU and FPGA combination would be an ideal solution by utilizing best of both worlds. But FPGA development is more complex and often hard to achieve time-to-market requirements.
Xilinx developed a hard- and software-based ecosystem to utilize FPGAs as a kind of remote processing element along with CPU. Xilinx' new unified software environment, called VITIS, offers the capabilities to integrate CPU code within FPGA kernels which helps to accelerate FPGA based development by staying in high level programming languages and using OpenCL API for application offloading and data path acceleration.
In this course, you will learn how to develop, debug, and profile new or existing C/C++ and RTL applications with VITIS targeting both data center (DC) and embedded applications. You will also learn how to run designs on the XILINX ALVEO accelerator board.

The course is focused on:

- Building a software application using the OpenCL™ API to run hardware kernels on Alveo accelerator cards
- Building a software application using the OpenCL API and the Linux-based Xilinx runtime (XRT) to schedule the hardware kernels and control data movement on an embedded processor platform
- Demonstrating the Vitis environment GUI flow and makefile flow for both DC and embedded applications
- Describing the Vitis platform execution model and XRT
- Describing kernel development using C/C++ and RTL
- Utilizing the Vitis analyzer tool to analyze reports
- Explaining the design methodology to optimize a design

usable technology

- Vitis unified software environment 2019.2
- Architecture: Xilinx Alveo accelerato-cards, (MP)SoCs and ACAPs

requirements

- Basic knowledge of Xilinx FPGA architecture
- Experience with the C/C++ programming language
- Software Development Flow

duration and cost

2 days, € 2.100,-

AGENDA

- Introduction to the VITIS Unified Software Platform
- Understanding Hardware Acceleration
- Processing offload vs Path optimization
- ALVEO Data Center Accelerator Cards Overview
- Getting Started with ALVEO Data Center Accelerator Cards
- Introduction to Nimbix Cloud
- VITIS Execution Model and XRT
- OpenCL Framework Fundamentals
- Xilinx OpenCL Synchronization Techniques
- Working with N-Dimensional Ranges (NDRanges)
- Profiling and Debugging
- Introduction to C/C++ based Kernels
- Using the RTL Kernel Wizard to Reuse Existing IP as Accelerators
- Optimizing the Performance of the Design for C/C++ based Kernel and Host Code
- VITIS Accelerated Libraries, BLAS, Fintech, and OpenCV
- Memory Transfer Optimization Techniques
- XDMA vs QDMA Data Flow
- VITIS analyzer tool to analyze reports
- Practical live demos based on XILINX ALVEO accelerator card

PLC2 TRAINING