

Workshop

Designing for Performance with XILINX FPGAs

This PLC2 workshop provides a comprehensive presentation of the latest XILINX FPGAs. Besides the architecture of the programmable devices the complete XILINX FPGA design flow as well as methods and procedures for efficient FPGA development build the main focus area. In particular, achieving the highest clock rates with high utilization ratios is often a major challenge in the development of FPGAs.

The use of specific timing constraints can be the key to success here. Timing constraints and their use is therefore one of the focal points of this workshop. The description language VHDL is already widely established in development departments. This workshop uses examples to show how VHDL is integrated in the design cycle, or rather which basic strategies should be followed in logic synthesis. Because VHDL itself is not taught in this workshop,

participants should already have a basic knowledge of it; for this we recommend the PLC2 workshops “Compact VHDL” and “Professional VHDL”. The theoretical content is complemented with PC based practical exercises.

Applicable technologies

Spartan6/ Virtex6

Requirements

Basic knowledge of XILINX FPGA architectures

Basic knowledge of VHDL

Fundamental knowledge of XILINX Design Tool Flow

Duration and Cost

Duration: 3 day

Cost: € 1.900, – net per person, including detailed training material, drinks in the breaks and lunch.

Agenda

Designing with FPGA Resources

- Introduction
- I/O
- Block RAMs and FIFOs
- DSP48 Resources

CoreGenerator Software System

- Overview
- Using the CoreGenerator Software System
- CoreGenerator Software Flow

FPGA Design Techniques

- Duplicating Flip-Flops
- Pipelining
- I/O Flip-Flops
- Synchronization Circuits

Introduction to Efficient Synthesis and Coding Tips

- Achieving Timing Closure
- Timing Reports
- Interpreting Timing Reports

Path-Specific Timing Constraints Part1

- Creating Groups
- Inter-Clock Domain Constraints
- Multi Cycle Path

Path-Specific Timing Constraints Part2

- False Path
- OFFSET Constraints
- Miscellaneous Constraints
- Advanced Implementation Options

Advanced MAP and Place & Route Options

- SmartXplorer
- SmartGuide Technology

PC based Exercises