

Workshop

XILINX Partial Reconfiguration

New

Partial Reconfiguration is a new option for the XILINX FPGA development tool suite.

Using this technique the FPGA development can be managed in independent teams for a particular region within the FPGA. Modular designs could be exchanged in the field or features could be multiplexed in partial reconfiguration bitstreams to use a smaller FPGA device for cost reduction.

During runtime partial configuration files can be loaded into the FPGA while other modules, like a MicroBlaze processor i.e. are working uninterrupted.

This course demonstrates how to use the ISE, PlanAhead, and Embedded Development Kit (EDK) software tools to construct, implement, and download a Partially Reconfigurable (PR) FPGA design.

The students will gain a firm understanding of PR technology and learn how successful PR designs are completed.

They will also identify best design practices and understand the subtleties of the PR design flow. The various configuration methods (JTAG, SelectMap, Flash) are used in practise during the workshop and the students obtain hints and tips on performance and resource optimization.

Applicable technologies

Virtex-5, Virtex-6, Virtex-7 FPGAs

Requirements

Good knowledge of XILINX FPGA Architecture and Tool Flow

Recommended knowledge: MicroBlaze, PlanAhead

Duration and Cost

Duration: 2 days

Cost: € 1.350, – net per person, including detailed training material, drinks in the breaks and lunch.

Agenda

Partial Reconfiguration Methodology

- Overview
- PR Terminology
- PR Design Flow

Partial Reconfiguration Design Recommendations

- Design Requirements and Guidelines
- Design Recommendations
- PR Tool Flow

Partial Reconfiguration Tool Flow

- PR Flow Details
- Scripted Flow

FPGA Configuration Overview

- Introduction to Configuration
- Configuration Modes
- Configuration Process

Partial Reconfiguration Bitstreams

- Bitstream Integrity
- ICAP Silicon Resource

Managing Clock Resources

- Global Clocks
- Regional Clocks
- I/O Clocks

Managing Timing

- Timing
- Timing Constraints
- Timing Analysis
- Simulation

Partial Reconfiguration Debugging

- General Debug
- ChipScope Pro Debugging

PCIe Core and Partial Reconfiguration

- Partial Bitstream Booting
- PCIe Core Bitstream Loading

Labs

- Partial Reconfiguration Flow
- Building an HDL ICAP Controller
- Partial Reconfiguration Timing Analysis and Constraints
- EDK Partial Reconfiguration