

## Workshop Compact Verilog

The continuously rising demand for highly complex programmable logic in combination with ever increasing clock rates creates new challenges for the users. Speed, flexibility and highest quality results are crucial factors for the economic success of a company. To achieve these goals, users must adopt modern and powerful hardware description language (HDL) based design techniques. A shortening of the development time as well as high quality designs can both be obtained with a Verilog based approach.

The PLC2 workshop “Compact Verilog” teaches the participant the Verilog syntax and its usage. The attendee learns the basic description elements as well as the application areas of this hardware programming language. The theoretical content is complemented with PC based exercises. For synthesis and simulation a maximum of two participants work together at one PC. During a series of labs

the participants will describe multiple Verilog modules that build together a complex design. The development cycle will be completed by implementing and porting this onto the provided FPGA evaluation board, thus allowing to also learn about the configuration mechanism and to test the loaded design on real hardware.

### Applicable technologies

All (technology independent)

### Requirements

Basic knowledge of digital technology (as taught in e.g. “Compact FPGA Design Techniques”) is helpful

### Duration and Cost

Duration: 3 days

Cost: € 1.900, – net per person, including detailed training material, drinks in the breaks and lunch.

## Agenda

### The XILINX Design Tool Flow

### Application and Deployment Areas of Verilog

- The concept of Verilog language

### The Verilog Design Flow

- Design Entry with Verilog
- Syntax and Instruction
  - Overview
  - Operators
  - Building hierarchical Structures
  - Procedural Blocks
  - Blocking vs. Non-Blocking Statements
  - Functions and Tasks
  - Compiler Directives

- The use of core generators and IP-Cores
- Verilog coding hints for FPGAs

### The Verilog Synthesis

- Coding Style: Combinatorial Logic
- Coding Style: Clocked Logic

### Description of Complex Circuits in Verilog

- development of applications followed by testing in real hardware

### The Verilog Simulation

- The Verilog test fixture concept and the process of simulation

### PC based Exercises