

Workshop

Advanced Synthesis with XST

Besides the physical implementation of integrated circuits, Synthesis is one of the most important steps in the design flow of FPGAs. Even though the synthesis process is largely automated and delivering efficient results in many cases, there are still situations in which the developer is required to intervene. This is especially true for high speed designs and/or high integration densities.

The Workshop “Advanced Synthesis with XST” covers both fundamental synthesis techniques for combinatorial and clocked circuits and more advanced techniques that are based on specific attributes.

“Advanced Synthesis with XST” is conceived for developers which already have some level of experience in designing for FPGAs. The ideas of the examples discussed during

this workshop are applicable to all XILINX FPGA families.

Applicable technologies

All XILINX FPGA technologies

Requirements

Ease in using VHDL programming language

Familiarity with FPGAs and XILINX design tool flow

Duration and Cost

Duration: 2 days

Cost: € 1.350, – net per person, including detailed training material, drinks in the breaks and lunch.

Agenda

XST VHDL Coding Techniques

- Comparator
- FF/Latch
- SRL
- Counter
- ROM/RAM
- DDR-Resources
- Finite State Machine (FSM)

Reading Synthesis Report

XST Synthesis Options

- Register Duplication
- Register Balancing

- Resource Sharing
- FSM options
 - Encoding Algorithm/Style
 - Safe Implementation
 - FSM in BlockRAM
- ROM/RAM Style
 - distributed
 - block
- Asynchronous to Synchronous

Synthesis Constraints (Attribute and XCF)

- Project wide settings
- Module level settings
- Signal specific settings