

Workshop Advanced PlanAhead

Being a powerful analysis and floorplanning tool, PlanAhead nowadays is packaged with all versions of the ISE software. It gets continuously developed towards an alternative to the project navigator most likely replacing it a day. At the same time, PlanAhead is the key to partial reconfiguration.

The workshop “Advanced PlanAhead” teaches the participant ways of detailed interventions using the PlanAhead software to implement FPGA circuits successfully. Building up on the skills taught in the class “Essential PlanAhead”, this course stresses area constraints via pblocks (physical blocks) and in conjunction with that the floorplanning of an FPGA. In this context, amongst others, location constraints for primitives are covered as well as re-using results of previous implementation attempts or working with partitions. Even ChipScope Pro is directly available and it will be shown how to take advan-

tage of this tight integration. In this context, choosing the signals to be probed and configuring the necessary core cells (ICON and ILA) are discussed.

For better familiarisation, multiple PC based exercises on provided designs are performed.

Applicable technologies

Recent FPGA technologies

Requirements

Detailed knowledge of FPGA technology and the XILINX Design Tool Flow

“Essential PlanAhead” is recommended

Duration and Cost

Duration: 2 days

Cost: € 1.350, – net per person, including detailed training material, drinks in the breaks and lunch

Agenda

PlanAhead Software Review

RTL Development and Analysis

- RTL Design Flow Review
- Exploring the Logic Hierarchy
- Viewing the RTL Schematic
- Analyzing Resource Estimates

Placing Dedicated Resources

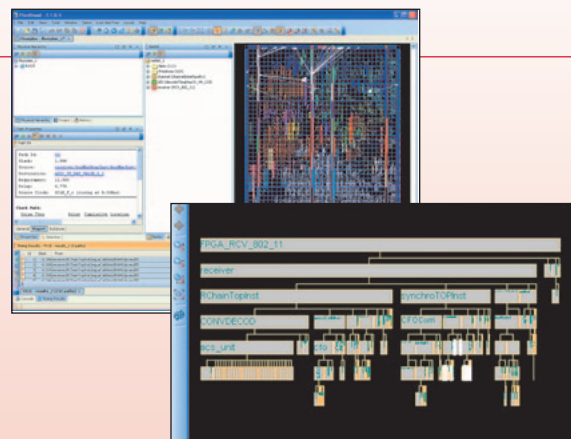
- What is Floorplanning?
- Making Placement Constraints

Pblocks

- Why Floorplan?
- Design and Synthesis Recommendations
- Pblocks
- Floorplanning Tools

Floorplanning Techniques

- Floorplanning Principles
- Floorplanning Methodologies
- Case Study
- Additional Floorplanning Tips



Design Preservation with Partitions

- Reasons for Partitioning
- Setting Up for Partitions

Debugging with the ChipScope Pro Tool

- ChipScope Pro Tool Integration
- Selecting Signals for Debugging
- Configuring ChipScope Pro Tool Cores
- Implementing ChipScope Pro Tool Cores
- Launching the ChipScope Pro Analyzer