

PowerWorkshop

Professional PCI Express

The availability of the Spartan-6/ Virtex-6 families enables effective PCIe Express (PCIe) solutions especially when taking advantage of the built-in IP cores.

The workshop starts introducing common terms and definitions before detailed information about the protocol and data packet construction is given. This way, the participant is skilled for implementing custom applications. Progressing, the class emphasizes the verification of a sample design through simulation which ensures the best possible coherence between the learning and a real world scenario which in return assures easy re-use of taught skills. Special attention is paid to the AXI interface constituting the link between the core cell and the user application part of the design. The relevant signals along with their meaning are discussed in a detailed fashion.

During the course, the target technology is Spartan-6.

However, the basic idea of the skills learnt applies to other architectures, too.

More than the workshop “Designing with PCIe” this class stresses practical experience.

Applicable technologies

Spartan-6 and Virtex-6 FPGAs (Virtex-5, too)

Requirements

Basic knowledge of VHDL

Basic knowledge of XILINX Design Tool Flow

Basic knowledge of Spartan-6/ Virtex-6 Architecture

Duration and Cost

Duration: 5 days

Cost: € 2.900, – net per person, including detailed training material, drinks in the breaks and lunch.

Agenda

Introduction to PCI Express

- PCIe Basics
- Topology
- PCIe Standards: Gen1 & Gen2

PCIe Layers

- Architecture
- Transaction Layer
- Data Link Layer
- Physical Layer

PCIe User Interface

- Transaction Types
- TLP Fields
- Packet Routing
- TLP Requests and Completion Packets
- AXI Interface

PCIe Initialization and Configuration

- Configuration Mechanisms
- Configuration Registers
- Configuration Capabilities

XILINX PCIe Solutions

- Soft Cores
- Embedded Cores

PCIe Usage

- CoreGen Wizards
- PCIe Implementation and Simulation
- Handling Interrupts and Errors
- Handling Power Management

PCIe Design Example

- Application Example

Labs

- Constructing the Endpoint Core
- Downstream Port Model Simulation
- Pseudo-Transactional Modeling
- Design Implementation
- Debugging the PCIe Core with the ChipScope Pro Tools