

Workshop

High-Speed Memory Interfacing

The new Xilinx FPGA families Spartan-6 and Virtex-6 offer very fast interfaces to external memories. Both families have new IOBs inside the FPGAs. The new CoreGen wizards generate the memory controller. This results in shifting of realization challenges from FPGA level to board level. The very high data rates require special care in the board design domain.

The 2-day workshop “High-Speed Memory Interfacing” targets to FPGA designers, as well as to System Architects and Layout designers, who want to implement fast memory interfaces and to use them in a system.

This workshop explains the options of the IOBs for memory interfaces. In result of this, the students learn how to use these options in interaction with the PCB design. Solution for signal integrity problems will be discussed: mainly signal quality and timing, but also power supply.

Hardware with DDR2 / DDR3 memories is used in this workshop to explain design and verification examples from praxis. Simulation options will be discussed.

Moreover, rules for successful realisation of memory interfaces will be commented on.

Applicable technologies

Spartan-6 and Virtex-6, older FPGA families on demand

Requirements

Basic knowledge on VHDL and FPGA implementation

Duration and Cost

Duration: 2 days

Cost: € 1.350, – net per person, including detailed training material, drinks in the breaks and lunch.

Agenda

Introduction

- Spartan-6 / Virtex-6 technology overview
- Memory solutions overview
- DDR2 / DDR3 standard
- Write / read leveling

Logical Design

- Usage of the XILINX resources
- Options and challenges
- Design parameters

Physical Design

- PCB design parameters
- PCB design requirements
- Board-Level simulations
- PCB design rules
- Power supply

System Analysis

- FPGA timing analysis
- PCB timing analysis
- System timing analysis
- Design parameter optimization
- Summarizing all design rules

Test and Debugging

- Functional verification
- Options and strategies for debugging

Labs:

- Controller design
- Logic simulation memory interface
- Timing analysis memory interface
- Test and verification DDR2 / DDR3 memory interface
- Verification physical layer by simulation (reflection and crosstalk)
- Verification physical layer by hardware (boards with DDR2 / DDR3 memories)