

PowerWorkshop

Expert DSP Design using System Generator

This PowerWorkshop is intended for FPGA developers using the Mathworks Simulink environment for FPGA development.

It is designed for FPGA developers who already have experience of DSP. After a brief overview of toolchain and the architectural features of XILINX FPGAs that are especially important for DSP applications, you will learn how complex DSP applications can be efficiently implemented in FPGAs using the XILINX System Generator.

A focal point is the use of the design system Matlab, in combination with the System Generator, another point is the HDL based project management using the XILINX IDE. In the broad-based practical part you will describe on your own complex circuits from all kinds of DSP application areas with Matlab/System Generator and verify them with Simulink an/or HDL simulation. After the concluding implementation, you will verify the correct

functioning of these circuits by porting them onto real systems/test boards. Each participant will be given all the necessary equipment such as the development computer and evaluation hardware. This gives them the best possible idea of the real and practical job of the developer. Naturally you can also work on concrete assignments as part of the practical section.

Applicable technologies

XILINX FPGAs

Requirements

Knowledge of digital signal processing.

Duration and Cost

Duration: 5 days

Cost: € 2.900, – net per person, including detailed training material, drinks in the breaks and lunch.

Agenda

Matlab Simulink Basics

- Stimulus and Response
- Sampling and Resolution
- Design Hierarchy and Subsystems

XILINX System-Generator Basics

- Interfacing and Data Types
- Constructing the Design
- System-Generator Blockset

Digital Filter Implementations

- FIR Filters
- IIR Filters
- Distributed Arithmetic Filters
- Parallel Filters
- Sequential Filters
- Semi-parallel Filters
- FFT Filters

Verification

- Simulink Verification
- HDL Co-Simulation
- Hardware Verification
- Testbench Verification

Signals in System-Generator

- Signal Conversion
- Signal Extraction
- Expression Blocks

Implementing System Control

- Control Mechanisms

- Block Operations
- Implementing .m File Functions

Micro Controllers

- PicoBlaze in Simulink
- MicroBlaze and PowerPC
- Creating CoProcessors

Multi-Rate Systems

- Sample Rate Conversion
- Sample Rate Changing Blocks
- Simulink Propagation Rules
- Timing Constraints

DSP Macro Programmierung

- DSP48: Programming the Core
- Pipelining an Algorithm

Creating Various Submodules for ISE

- File Structure
- HDL Flow, Netlist Flow
- Simulation Flow
- Timing and Area Constraining

Designing with Shared Memories

- Memories, Shared Memories
- Register based Interfaces
- BlockRAMs and FIFOs

Achieving Higher Performance

- Timing Analysis Compilation
- Performance Improvements