XILINX®

XPERTS XILINX Program for Engineering Resources from Third Parties

PLC2 PROGRAMMABLE LOGIC COMPETENCE CENTER

Workshop
Designing with Multi-Gigabit Serial I/O

The new Spartan-6 and Virtex-6 platforms allow serial interfaces in the Gbit/s range. This involves the use of new transceivers, which require comprehensive know-how for quick and effective use. The 3-day PLC2 workshop "Designing with Multi-Gigabit Serial I/O" is aimed at developers who want to implement serial interfaces in the Gbit/s range and use them in a system. This workshop enables developers to effectively use all available features of the RocketI/Os, define the interfaces and attributes necessary for the features, and instantiate the RocketI/O primitives with the Architecture Wizard integrated in the CoreGenerator, in order to implement project-specific interfaces or standardized serial interfaces. The Serial I/O Toolkit for ChipScope is used to show an effective verification of the serial transmission link. Signal-integrity topics, including a simulation example and pointers on board design, provide practical tips for implementation.

Applicable technologies

Spartan-6 and Virtex-6 FPGAs

Requirements

Basic knowledge of VHDL and FPGA Implementation

Duration and Cost

Duration: 3 day

Cost: € 1.900, – net per person, including detailed training material, drinks in the breaks and lunch.

Agenda

Introduction

- Spartan-6 / Virtex-6 technology overview
- GTP overview
- GTX overview
- GTH overview

Clocking, timing and RESET

Physical Coding Sublayer

- Fabric interface
- Encoding / decoding
- Symbol alignment, clock correction
- Channel bonding

Physical Media Attachment

- Serial IO
- Pre-Emphasis and equalization

Implementation and Verification

- Architecture Wizard
- SecureIP simulation
- ChipScope IBERT design

System Design

- 64B/66B and 64B/67B encoding and the Gearbox
- PMA Layer details
- Boarddesign
- Link optimization
- Test and debugging

Labs:

- Coding/encoding lab
- Using Commas and K-character symbols
- Clock correction
- Channel bonding
- Using Architecture Wizard
- Implementation and Simulation
- 64B/66B encoding
- System-Lab: from Planning to Debugging / Link Optimization