

Workshop Timing Constraints

Developing complex FPGAs with demanding timing standards often requires procedures such as floorplanning, Relationally Placed Macros (RPM), and incremental design, but with special Time-driven implementation procedures (timing constraints). The 2-day PLC2 workshop “Timing Constraints” concentrates on such timing constraints and is aimed at FPGA designers who already have a sound basic knowledge of XILINX FPGA development. After the detailed presentation of the TRACE tool used for Static Timing Analysis typical timing errors and their cause will be analyzed. In addition to this, participant will learn the methods to correct these errors. Based on the “Timing Closure” strategy developed by XILINX total available bandwidth of existing timing constraints will be presented. The next topic discusses the Global timing constraints on the simple and synchronous circuits. Next

we will see the definition of complex paths like multicycle constraints, false path in general circuits. Furthermore there is also a possibility to enter these timing constraints using XILINX Constraints Editor basically which is an effective method of entering the Timing Specification in the UCF file.

Applicable technologies

All kind of FPGA technologies

Requirements

Detailed knowledge of the ISE design system

Duration and Cost

Duration: 2 days

Cost: € 1300, – net per person, including detailed training material, drinks in the breaks and lunch.

Agenda

Timing budget

- Basic model
- Input / Output Timing
- Optimization of clock frequency
- Pipelining
- Multicycle

XILINX Timing Closure Flow

Timing Analyzer

Common Timing Errors

- Interpreting Timing Reports

Basic Constraints

- PERIOD Constraint
- OFFSET Constraint
- DUTY_CYCLE
- MAX_DELAY
- TIG
- OFFSET

XST timing constraints

- Introduction
- XST timing constraints
- Timing model
- Priority

UCF/NCF FILES

- Introduction
- UCF Flow
- UCF/NCF File Syntax
- Common Constraints
- Path-Specific Constraints

The Constraints Editor

- Creating Groups
- Creating OFFSET IN/OUT Groups
- Inter-clock Domain Constraining
- Constraining Multi-cycle Paths
- False Paths
- Miscellaneous Options

Constraint Priority

Advanced Timing Constraints with the UCF File

- FROM: TO and Groups
- Groups with TNM
- More on Groups
- TPTHU and TPSYNC
- TIG
- MAXDELAY and MAXSKEW
- DCM Constraints