

Workshop Signal Integrity

The new XILINX FPGA families allow interfaces with high clock and data rates, in which the developer is forced to allow for the effects of signal integrity. The 3-day PLC2 workshop “Signal Integrity for XILINX FPGAs” is aimed at developers who want to implement high-speed interfaces between a XILINX FPGA and other components. Participants are taught to judge when the signal integrity needs to be taken into account. For further analysis, IBIS models, for example, are available, the use and creation of which is described. These models form the basis for advanced analyses (reflections, crosstalk, etc.) with HyperLynx. Based on these basic analyses, participants learn how to simulate complex interfaces, for example 333MHz

memory interfacing. The simulation of the serial interfaces is based on various design kits, whose design-specific adaptation is shown with a lab.

Applicable technologies

SPARTAN-3 Families, Virtex-4, Virtex-5

Requirements

Basic Knowledge and VHDL implementation

Duration and Cost

Duration: 3 day

Cost: € 1850, – net per person, including detailed training material, drinks in the breaks and lunch.

Agenda

Introduction and Architecture

- Virtex technology overview
- Spartan technology overview
- Clocking Resources
- SelectIO and serial interfaces
- Packaging
- Configuration overview

Transmission Lines

- Basics
- Critical trace length

IBIS Models and SI Tools

- IBIS standard
- IBIS editor
- XILINX IBIS models
- SI tools
- HyperLynx

Reflections and Crosstalk

- Reflection effects and calculation
- Minimizing reflections: trace termination
- Crosstalk effects and calculations
- Minimizing crosstalk

Signal Integrity Analysis

- Methods
- Modeling of components
- System analysis:
 - High-speed memory interfaces
 - RocketIO MGT – GTP/GTX

Power Supply

- Impedance – inductance
- Bypassing

Technology Specific Solutions

- Powering
- Signal interfacing
- Packaging and thermal aspects

Labs

- Invoking HyperLynx
- Analysis of reflection effects
- Analysis of crosstalk effects
- Memory interface example
- Serial I/O example