

PowerWorkshop

Professional XILINX Design Constraints

The performance requirement for FPGA development is rising steadily. There are many factors which are responsible for the FPGA performance e.g. Circuit design techniques play an important role in FPGA's performance. These circuit design techniques are discussed in brief in PLC2 other workshops called as "Compact FPGA Schaltungstechnik" and "Professional FPGA Schaltungstechnik". Basically Timing Constraints and Physical Constraints are two very important components for the FPGA development. Physical Constraints consist of many approaches such as "Floor-Planning", "relationally placed macros (RPM's)", "incremental/modular design" and also have other techniques to optimize the layouts of the FPGA. This topic includes other Constraints also like Pinout Constraints, Area Constraints and optimization strategies like Smart Guide and Smart Compile. In the timing constraint section, we will discuss in brief the Static Timing Analysis, Trace Tool, typical timing

errors and their causes. This topic also includes the global timing Constraints on simple synchronous circuits and definition of complex technical paths in general circuits, such as Multi-Cycle Constraints, False Path.

The 5-days power workshop "Professional XILINX Design Constraints" is focus on the procedures for optimizing the FPGA design and gives FPGA designer a solid knowledge of XILINX FPGA based design.

Applicable technologies

All kind of FPGA technologies

Requirements

Detailed knowledge of the ISE design system

Duration and Cost

Duration: 5 days

Cost: € 2.700, – net per person, including detailed training material, drinks in the breaks and lunch.

Agenda

Timing budget of digital Circuits

- Basic model
- Input / output Timing
- Optimization of clock frequency
- Pipelining & Multicycle

Timing Analyzer

- Interpreting Timing Reports

Basic Constraints

- PERIOD Constraint
- OFFSET Constraint
- DUTY_CYCLE
- MAX_DELAY

XST timing constraints

- XST timing constraints
- Timing model

UCF/NCF FILES

- UCF Flow
- UCF/NCF File Syntax
- Common Constraints
- Path-Specific Constraints

The Constraints Editor

- Creating Groups
- Inter-clock Domain Constraining

- Constraining Multi-cycle Paths
- False Paths
- Miscellaneous Options

Advanced Timing Constraints with the UCF File

- FROM: TO and Groups
- Groups with TNM
- More on Groups
- TPTHU and TPSYNC
- TIG, MAXDELAY and MAXSKEW

Physical constraints

- Options for map
- Options for place and route

Floor planning

- Area constraints and I/O layout
- Floorplanner
- PlanAhead

FPGA Editor

- FPGA Editor Basics

Smart Guide

SmartCompile