XILINX®

XPERTS
XILINX Program for Engineering Resources from Third Parties

PLC2
Programmable Logic Competence Center

Workshop Physical Constraints

The performance requirements for FPGA development is rising steadily, there are many factors which affect the performance of FPGA. First is the circuit design technique which plays a major role in FPGA performance. Secondly, timing constraints which are equally important component for the FPGA development. These two factors are discussed in brief in PLC2 other workshops like "timing constraints" and "FPGA Schaltungstechnik ". The other essential aspects of FPGA development are physical constraints. This includes various approaches and strategies e.g. "Floorplanning", "relationally placed macros (RPM)", "incremental/module design" and other special techniques to optimize the FPGA layouts. The 2-days workshop on "physical constraints" focus on all these mentioned factors to optimize the FPGA layout and provide FPGA designer a solid Xilinx FPGA based design knowledge.

Based on Xilinx FPGA flow the option for MAP and PAR will be discussed in detail. Then examples on PACE, Floorplanner and PLAN AHEAD will be presented. After this very important constraints like pinout constraints, area constraints and optimization strategies smart guide and smart guide will be discuss in brief. Furthermore the optimization of FPGA with FPGA Editor will be explained. Beside the possibility of entering the constraints with the Xilinx pinout and area constraints Editor (PACE) the constraints can also entered directly to the UCF file which is also an efficient method of entering the constraints.

Applicable technologies

All kind of FPGA technologies

Requirements

Basic knowledge of digital technology (e.g. Compact FPGA Schaltungstechnik)

Duration and Cost

Duration: 2 days
Cost: € 1.300, – net per person, including detailed training material, drinks in the breaks and lunch.

Agenda

Introduction
- Options for map
  - Physical
  - Timing
- Options for place and route
  - Physical
  - Timing

Basic floor planning
- Introduction
- Area constraints and I/O layout
- Floorplanner

Advanced floor planning
- Introduction
- RPM

FPGA Editor
- FPGA Editor Basics
- Viewing Device resource and constrained paths
- In-circuit testing

Methods for optimizing
- Smart Guide
  - Introduction
  - Smart Guide
  - Partitions
- SmartCompile
  - SmartCompile-XST
  - SmartCompile-Synplify pro

PLAN AHEAD
- Design analysis
- Partitioning and floor planning
- Implementation