

Workshop XILINX FPGA Configuration

Configuring Xilinx FPGAs is the topic of this new course. Configuration specific knowledge is not required in order to successfully complete the course. Starting with basic background information, the different configuration modes are presented. This enables the designer to make the good choice when choosing the configuration mode for his application. The JTAG interface and its usage for configuration and verification are discussed. Furthermore PROMs and respective application tips, generating files for usage in conjunction with automated test equipment, SystemACE and the Spartan3E specific configuration modes SPI and BPI will be covered. Exercises help to get a better understanding for the content.

Applicable technologies

Virtex Series, Spartan Series

Requirements

Detailed knowledge of FPGA technology and ISE design flow

Duration and Cost

Duration: 2 days

Cost: € 1300, – net per person, including detailed training material, drinks in the breaks and lunch.

Agenda

Knowledge about configuration

- Configuration course
- Configuration modes

Serial/Parallel configuration

- Interface
- Waveform diagram
- Debugging
- Exercises

JTAG and SVF

- JTAG for configuration, readback and verification
- Internal registers
- BSDL
- SVF commands and generating files

PROMs

- Presentation of the PROM families
- Data compression and encryption

SystemACE

- Presenting the solution
- Managing multiple bit stream versions
- Microcontroller interface

SPI/BPI

Cheat Sheet

Exercises on the PC and with evaluation board

