

PowerWorkshop Expert FPGA

The development of complex FPGAs with demanding timing standards requires special procedures such as floorplanning, Relationally Placed Macros (RPM), and incremental design. Although uses of the graphical design interface Foundation ISE, for example, also allows fast and clear FPGA development, it does not support all available options. This 5-day PowerWorkshop concentrates on advanced FPGA design techniques and is aimed at FPGA designers who already have a sound basic knowledge in the field of XILINX FPGA development. Topics covered include scripting techniques and implementation via command lines, modifications and probes with the FPGA editor, generation and use of RPMs, and Floorplanner and incremental design techniques. The theoretical basics are rounded off with intensive exercises on the PC.

Applicable technologies

All FPGA Technologies

Requirements

Basic architecture of an FPGA (Spartan Virtex) would be helpful detailed knowledge of the ISE design system

Duration and Cost

Duration: 5 days

Cost: € 2700, – net per person, including detailed training material, drinks in the breaks and lunch.

Agenda

Timing Closure Flow

Achieving Timing Closure

Advanced Implementation Control

Tcl Scripting

- Introduction
- Managing Projects
- Setting and Inspecting Properties
- Design Implementation and Analysis
- Advanced Scripting

UCF Editing

- Introduction
- Common Constraints
- Path-Specific Constraints
- Additional Constraints
- Constraint Priority

Advanced I/O Timing

- Timing Introduction
- Input Timing and Constraints
- Output Timing and Constraints

SmartCompile Design Preservation Techniques

- Introduction

- SmartGuide
- Partitions

Floorplanning Effective Layout

- Introduction
- Area Constraints and I/O Layout
- Floorplanner
- PlanAhead

Reduce Debug Time

- FPGA Editor: Viewing and Editing a Routed Design
- FPGA Editor Basics
- Viewing Device Resources and Constrained Path
- In-Circuit Testing

Lab 1: Achieving Timing Closure

Lab 2: Tcl Scripting

Quick Reference: UCF Common Constraints

Lab 4: Advanced I/O Timing

- System Synchronous SDR Interface
- Source Synchronous DDR Interface

Lab 5: SmartCompile