

## Workshop

# Designing for Performance with XILINX FPGAs

This PLC2 workshop provides a comprehensive presentation of the latest XILINX FPGAs. As well as the architecture of programmable modules, it concentrates on the complete XILINX FPGA design flow as well as methods and procedures for efficient FPGA development. In particular, achieving the highest clock rates with simultaneous high utilization is often a major challenge in the development of FPGAs. The use of specific timing constraints can be the key to success here. Timing constraints and their use is therefore one of the focal points of this workshop. The description language VHDL is already widely established in development departments. This workshop uses examples to show how VHDL is integrated in the design cycle, or rather which basic strategies should be followed in logic synthesis. Because VHDL itself is not

taught in this workshop, participants should already have a basic knowledge of it; for this we recommend the PLC2 workshops “Compact VHDL” and “Professional VHDL”. The theoretical content is rounded off with practical exercises on the laptop/PC.

### Applicable technologies

Spartan3 / Virtex-4 / Virtex-5

### Requirements

Basic architecture of an FPGA (Spartan 3 / Virtex derivatives) would be helpful, detailed knowledge of the ISE design system

### Duration and Cost

Cost: € 1850, – net per person, including detailed training material, drinks in the breaks and lunch.

## Agenda

### Introduction to XILINX Products

- XILINX Hardware & XILINX Software

### Basic Virtex/Virtex-II Architecture

- CLB Resources & I/O Resources
- Memory, Multipliers & Clock Resources

### Reading Overview and reading Reports

- Map Reports, Place & Route Reports, Timing Reports

### FPGA Design Techniques

- Hierarchy & Synchronous Design for XILINX FPGAs

### Introduction to Efficient Synthesis and Coding Tips

- Introduction to Synthesis
- Synthesis Tips & Coding Tips

### Global Timing Constraints & Advanced Timing Constraints

- PERIOD Constraint, OFFSET Constraint, Constraints Editor
- Timing groups & multi cycle

### Implementation Options

- Basic Software Options & Accessing Advanced Software Options

### Exercises on PC