

Workshop Compact FPGA Virtex Series

With the availability of virtex-5 family the effective implementation of large complex design is possible. The 3-days workshop “Compact FPGA Virtex Series” teaches the participant the new available features and design resources in the Virtex-5 FPGA. The focus of the workshop is on the description of basic architectural elements of all Virtex-5 families and their optimal implementation with VHDL. In addition to this software support by Core Generator and Architectural Wizard will be explained. A brief introduction on the specific features such as DSP48, Serial I/O and Embedded IP’s will be given. These special features are explained deeply in the PLC2 other workshop called as “Professional FPGA”. The basic command of VHDL and general approach to VHDL implementation of FPGA design is not the part of this workshop. The com-

mand on VHDL language can be achieved by attending PLC2 workshops like “Professional VHDL” and “Compact VHDL”. The theoretical content will be explained practically on PC. In the final section of the workshop an example will be implemented and tested in the real hardware (Xilinx evaluation board with Virtex-5 FPGA).

Applicable technologies

Virtex-5

Requirements

Basic knowledge of digital technology and VHDL.

Duration and Cost

Cost: € 1800, – net per person, including detailed training material, drinks in the breaks and lunch.

Agenda

Introduction Virtex-5 Technology

- Virtex-5 Platforms

Introduction ISE Design-Software

- Project management
- Design Entry
- Synthesis and verification
- Implementation

Clocking Resources

- Clock Manager Technology
- DCM
- Phase Lock Loops
- Global and regional clock networks
- Application examples

I/O Resources

- SelectIO resource: IOB
- SelectIO logic resources: ILOGIC, OLOGIC, IODELAY, IDELAYCTRL
- SelectIO advanced logic resources : ISERDES, OSERDES
- New I/O standards

Core Resources and Embedded Blocks

- 6-input LUT
- CLB
- Connectivity
- Distributed memories
- RAMB36: Block RAM application examples and Block RAM ECC
- FIFO36 and application examples
- Overview: DSP48E, embedded cores, serial I/O

Configuration Overview

Labs

- ISE design example
- DCM clocking
- PLL implementation
- OSERDES/ISERDES
- Core resources: 6-input LUT
- RAM/FIFO
- Design, verification and implementation of an application example using ISE