

Workshop

Compact FPGA Spartan Series

The 3-days workshop from PLC2 named as „compact FPGA Spartan Series“ teaches the new features and the use of available design resources of Spartan-3 FPGA. This workshop mainly focuses on architecture element of all Spartan-3 derivatives and its optimal implementation with VHDL. The development environment ISE will be discussed in brief. Additionally the software tools like System Generator and Architecture Wizard will be explained. The basic commands of description language VHDL and the general approach for implementation of FPGA design are not the part of this workshop. The VHDL basic can be learned in other PLC2 workshops like “Compact VHDL” and “Professional VHDL”. The Practical exercises will be

performed on PC. In the final part of the workshop an example will be implemented and tested in real hardware (XILINX evaluation board).

Applicable technologies

Spartan-3 Series

Requirements

Basic knowledge of VHDL and digital technology are helpful

Duration and Cost

Duration: 3 days

Cost: € 1.800, – net per person, including detailed training material, drinks in the breaks and lunch.

Agenda

The architecture of the Spartan-3 FPGAs

- IOBs
- CLBs (LUT, SRL16, distributed RAM)
- BlockRAM
- Clocking (IBUFG, DCM, BUFGMUX)
- Carry und Arithmetic Logic

Introduction to the ISE design software

- Project Management
- Design entry
- Implementation

Implementation Options

- Synthesis
- MAP
- PLACE AND ROUTE

I/O Resources

- SelectIO resource: IOB
- I/O standards
- Differential Signaling

VHDL Synthesis

- VHDL Coding Tips

Configuration Overview

- Configuration
- Relevant pins
- Implementation