

Workshop FPGA Board-Design

With the availability of the various XILINX FPGA families, both FPGA designers and layout Developers are faced with new implementation possibilities and challenges. All kinds of interfaces to External components enable a variety of application areas. The high clock rates accompanying the components require a comprehensive knowledge of physical design in the FPGA environment.

The 2-day PLC2 workshop “XILINX FPGA Board Design” train the designers in the practical use of XILINX FPGAs. It is aimed not only at VHDL developers who also have to integrate physical Interfaces of the FPGA, but also at design engineers and PCB layouters. The content covers the partly conflicting design restrictions of both design teams in order to show methods for effective Implementation of customer projects. Based on the FPGA power requirements (basics and power estimator), power-supply solutions (AC/DC or DC/DC converters,

filtering and decoupling) are presented. The termination required for high clock or data rates is covered in detail, taking into account different signal levels and termination variants. A special section deals with clock-pulse supply (strategies and implementation) and the connection to high-speed components on the board. Rules of PCB design (PCB tracing, layer stacking) are also explained.

Applicable technologies

SPARTAN-3 family, Virtex-4, Virtex-5

Requirements

Basic knowledge of VHDL and FPGA implementation

Duration and Cost

Duration: 2 days

Cost: € 1300, – net per person, including detailed training material, drinks in the breaks and lunch.

Agenda

Introduction and Architecture

- Virtex technologies overview
- Spartan technologies overview
- Clocking Resources
- SelectIO and serial interfaces
- Packaging
- Configuration overview

FPGA Power Supply

- Power estimation
- Power supply solutions
- Power filtering and decoupling

FPGA High-Speed Interfaces

- High-Speed signal standards
- Signal interfacing
- Transmission lines
- Combining I/O standards
- Signal coupling and translation
- SSO

FPGA Clocking

- High-Speed clock generation
- Clock distribution
- Board De-skewing

Physical Design, Modeling and Simulation

- PCB structures
- Trace characteristics
- Board design rules
- PCB modeling and simulation

Thermal Aspects

- Thermal resistance, modeling and calculation, heat sink selection

Labs

- I/O placement
- Power prediction
- Demo reflection and crosstalk using HyperLynx
- Thermal design