

Workshop Advanced FPGA Implementation

The development of complex FPGAs with demanding timing standards requires special procedures such as floorplanning, Relationally Placed Macros (RPM), and incremental design. Although the graphical design interfaces Foundation ISE allows fast and clear FPGA development, it does not support all available options. Also, the reproducibility functional designs (SmartCompile Design Preservation Techniques) are of great importance. The use of graphical design surface Foundation ISE is allow a quick and clear FPGA Implementation, but not supported for all available deployment options. Those options can either be accessed “command Line Interface” or with the help of TCL shell. The workshop “Advanced FPGA Implementation” focus on the advanced FPGA design techniques and useful for those FPGA developers who has solid basics in the field of XILINX FPGA development.

Topics included:

Scripting techniques and implementation of Command Lines, modifications and qualifications probe with the FPGA Editor, generation and use of RPMs and Floor Planner and incremental design techniques. The theoretical concepts will be explained practically on the PC.

Applicable technologies

All FPGA Technologies

Requirements

Basic architecture of an FPGA (Spartan Virtex) would be helpful detailed knowledge of the ISE design system

Duration and Cost

Duration: 3 day

Cost: € 1850, – net per person, including detailed training material, drinks in the breaks and lunch.

Agenda

Agenda Advanced FPGA Implementation

Timing Closure Flow

Achieving Timing Closure

Advanced Implementation Control

Tcl Scripting

- Introduction
- Managing Projects
- Setting and Inspecting Properties
- Design Implementation and Analysis
- Advanced Scripting

UCF Editing

- Introduction
- Common Constraints
- Path-Specific Constraints
- Additional Constraints
- Constraint Priority

SmartCompile Design Preservation Techniques

- Introduction
- SmartGuide
- Partitions

Floorplanning Effective Layout

- Introduction
- Area Constraints and I/O Layout
- Floorplanner
- PlanAhead

Reduce Debug Time

- FPGA Editor: Viewing and Editing a Routed Design
- FPGA Editor Basics
- Viewing Device Resources and Constrained Path
- In-Circuit Testing