

# Workshop PlanAhead

PlanAhead is a new software tool for analyzing and floor-planning FPGA designs. In the design flow it's situated between the synthesis and the translate process. Based on an existing netlist and implementation constraints communicated via UCF files, PlanAhead enables the engineer to optimize the layout in a graphical and intuitive manner. This results in better performance (timing) or higher packing density. Especially in high volume production this may lead to enormous cost reduction by using smaller FPGAs or devices of a slower speed grade. The incremental approach of PlanAhead leads to shorter run times of the implementation tools and keeps the results more consistent. For demonstration purposes and to gather a first experience, exercises are done using a real world example.

## Applicable technologies

Virtex Series, Spartan-3 Series

## Requirements

Detailed knowledge of FPGA technology and ISE design flow

## Duration and Cost

Duration: 2 days

Cost: € 1300, – net per person, including detailed training material, drinks in the breaks and lunch

## Agenda

### Application areas of PlanAhead

- High Performance Design
- High Density Design
- Incremental Design

### Design Analysis

- Importing netlists
- Design statistics, connectivity and timing

### Partitioning and Floorplanning

- Automated Partitioning
- Manual Partitioning
- Performance Improvements through Floorplanning

### Implementation

- Creating and Editing Constraints and Design Rule Checker (DRC)
- Importing Implementation results for further optimization

### Generation IP blocks

- Using incremental design techniques
- Exporting modules of IP

### Exercises on the PC

