

PowerWorkshop Expert VHDL

The 5-day PLC2 PowerWorkshop “Expert VHDL” is intended as an extension of the PLC2 PowerWorkshop “Professional VHDL” and likewise has a very high practical content. This PowerWorkshop is designed for FPGA developers who already have basic VHDL experience as well as a basic knowledge of the XILINX FPGA technology and want to develop and extend this knowledge further. One of the focal points of this PowerWorkshop is the verification of the module and the development of VHDL test benches.

After a comprehensive introduction to the verification concept offered by VHDL, in the board based practical part you will describe on your own complex circuits from all kinds of application areas as well as corresponding verification environments (test benches), and verify them with the VHDL Source Level Debugger/Simulator. The development of simulation models of external components needed for this is also included in the practical exercises. After the concluding synthesis, you will verify

the correct functioning of these circuits by porting them to real systems/test boards and you will check the signal responses forecast by the simulation environment. As well as the test board, each participant will be given all the necessary equipment such as a development computer with design software, power pack, signal generator and oscilloscope. This gives them the best possible idea of the real and practical job of the developer.

Naturally you can also work on concrete assignments as part of the practical section.

Applicable technologies

All CPLDs/FPGAS

Requirements

Basic knowledge of VHDL

Duration and Cost

Duration: 5 days

Cost: € 2700, – net per person, including detailed training material, drinks in the breaks and lunch.

Agenda

Review Basic VHDL

VHDL commands

Functions and Procedures Grinding

Verification tools for communication

- verification by high-level simulation
- Static Timing Analysis

Planning the verification communication

- Level Verification
- Verification Strategies
- response verification
- Timing Verification

Test Bench architectures

- Reusable components for the Verification
- Monitoring
- Intelligent Test Benches

Attributes and Generics

- signal types and attributes
- Reusable Components

Stimulus and Response

- Discrete, periodic and complex stimuli
- Analog stimulus
- Waveform Generators
- pseudo-random generators

File I / O

- File Read – Reading the stimuli from text files
- File Reviews – Issue of the results in Text files

Modelling external components

- AD converters
- DA converters
- memory

Exercises on the PC