

## Workshop

# Introduction to Assertion-Based Verification

**New**

In the development process of modern FPGA or ASIC designs, functional verification increasingly becomes the bottleneck of efficiency. A reduction of effort, time and cost of future HW developments can only be achieved through significant improvement of the verification methodology and automation.

This workshop practically introduces design, verification and integration engineers to industry wide trend for reducing verification effort: Assertion-Based Verification (ABV).

The most straight forward access to ABV delivering an immediate advantage is to use assertions in conjunction with formal verification tools. These tools allow for verification already in the RTL development phase. Thus, errors are found earlier while the effort for verification tasks still gets reduced significantly.

Based on real world examples, the participants learn to efficiently analyze and verify VHDL und Verilog design using System Verilog Assertions (SVA).

The practical exercises will use the 360MV verification tool developed by OneSpin (Munich).

### Applicable technologies

All (independent of technology)

### Requirements

Digital circuit design (RTL), Knowledge in VHDL and/or Verilog, basic knowledge in functional RTL verification is of advantage

### Duration and Cost

Duration: 2 days

Cost: € 1.350, – net per person, including detailed training material, drinks in the breaks and lunch.

## Agenda

### Assertion-Based Verification Basics

- What is Assertion-Based Verification (ABV)?
- Advantages and use cases of ABV
- Simulation based vs. ABV

### Automated RTL Analysis

- Identifying typical RTL coding errors
- Identifying discrepancies between Synthesis and Simulation results
- Identifying possibilities for design optimization

### Introduction to System-Verilog Assertions (SVA)

### Formal Verification of SystemVerilog Assertions

- Reading and Binding of SV Assertions
- Executing Assertions
- Interpretation of Verification Results

### Efficient Debugging of Assertions and RTL Designs

- Debugging Flow and Automisation
- Design Exploration

### Efficient RTL-Analysis and –Verification

- Use Examples for Design Engineers
- Use Examples for Verification Engineers

### PC based exercises based on real world designs