

Workshop Compact Verilog

With the constantly growing demand for highly-complex programmable modules combined with high clock rates, users are facing new challenges which are also constantly growing. Because speed, flexibility and a high level of quality are key to economic success, modern, powerful design methods based on hardware description languages must be used to satisfy the demand for the shortest development times and high quality. The 3-day PLC2 workshop “Compact Verilog” teaches you to use Verilog. You will get to know the basic description elements as well as the application areas of the language. The theoretical content is topped off with exercises on the PC. Each participant will have his own notebook with Verilog synthesis and Verilog simulation. As a final application example, you will de-

scribe and verify complex circuits in Verilog. In the concluding test, these circuits will be implemented and tested in real hardware (evaluation board).

Applicable technologies

All kind of FPGA technologies

Requirements

Basic knowledge of digital technology is helpful

Duration and Cost

Duration: 3 days

Cost: € 1800, – net per person, including detailed training material, drinks in the breaks and lunch.

Agenda

Application and deployment areas of Verilog

- The concept of Verilog language

The Verilog design flow

- with Verilog design entry
- syntax and instruction
 - Overview
 - Operators
 - Hierarchy Education
 - Blocking vs. Non-Blocking Statements
 - Functions and Procedures
 - Compiler directives
- The use of engine generators and IP Cores

The Verilog synthesis

- coding style: combinatorial logic
- coding style: clocked logic

Description of complex circuitry in Verilog

- development of applications with followed by testing in real hardware

The Verilog simulation

- The Verilog test the concept & Fixture Implementation of the simulation

Exercise participants on the PC