

Workshop Compact VHDL

By steadily rising demand for high complexity programmable logic combined with the high clock rates, growing new challenges for the users. Since speed flexibility and high quality are the crucial factor for the economic success. To cooperate with these factors user must adopt the modern and powerful hardware description language based design. The short development time and high quality design can be obtained with VHDL based designs. The 3-days workshop from PLC2 named as “Compact VHDL” trains the user with the use of VHDL. The participant learns the basic description element as well as application area of language. The theoretical content is rounded off with exercises on PC. Each participant will have a laptop with VHDL synthesis and VHDL simulation tools

on it. In the final section of the workshop, participant will describe and verify a complex design in VHDL and implement this design in real hardware (Xilinx evaluation Board).

Applicable technologies

All kind of FPGA technologies

Requirements

Basic knowledge of digital technology is helpful

Duration and Cost

Duration: 3 days

Cost: € 1800, – net per person, including detailed training material, drinks in the breaks and lunch.

Agenda

Application and deployment areas of VHDL

- The concept of VHDL language

The VHDL design flow

- Design Entry with VHDL
- Syntax and instruction
 - Overview
 - VHDL types
 - Processes
 - Operators
 - Concurrent and Sequential Statements
 - The use of core generators and IP-Core

The VHDL synthesis

- coding style: combinatorial logic
- coding style: clocked logic

Description of complex circuits in VHDL

- development of applications with followed by testing in real hardware

The VHDL simulation

- The VHDL test bench and the concept Implementation of the simulation

Exercise participants on the PC