

Workshop - ChipScope Integrierter Logic Analyzer for XILINX FPGAs

With increasing integration density of FPGAs the developer has less and less access to test points for measurements in order to verify his design in operation. A low number of I/O pins compared to the enormous amount of internal connections, cost and packing density of the PCB are the main criteria for a FPGA integrated logic analysis tool. With ChipScope, XILINX provides the option to probe FPGA internal signals and buffer them in on chip RAM. Via the hardware interface to the PC, the ChipScope software communicates with the hardware to be tested. This workshop demonstrates the possibilities of sophisticated FPGA verifications using ChipScope. Especially newcomers to VHDL can take advantage using this tool as an alternative to extensive HDL simulation in order to put a design in operation. A synthesis requirement is that adding cores does not influence the real time behavior. ChipScope cores are generated using real world designs. Afterwards they get tested using FPGA evaluation boards. Participants learn how the software part of the logic analyzer is organized and in which way known

features such as trigger menu and wave form representation of the data are available. Since processor internal bus signals can be displayed synchronized to the Debugger, this tool is especially interesting for embedded controller applications. Furthermore ChipScope offers the feature to accelerate HDL simulations by recording data from within the hardware and reusing the results for further simulation. Participants of this workshop learn to increase their efficiency in XILINX-FPGA design.

Applicable technologies

XILINX FPGAs

Requirements

Basic knowledge of XILINX FPGA Architecture and VHDL

Duration and Cost

Duration: 2 days

Cost: € 1.300, – net per person, including detailed training material, drinks in the breaks and lunch.

Agenda

ChipScope core and Tool Overview

- Supported FPGA families
- The chipScope tool flow

The chip Scope Core Generator

- The generation of icons
- The generation of different cores

Inserting the chipScope cores

- The possible options
- Flow based ISE

ChipScope in embedded applications

- Scope chip in microfinance projects Blaze
- PowerPC chip projects in Scope

ChipScope with Matlab and systemgenerator

- Chip generator system in Scope

Serial I / O Toolkit

ChipScope + Agilent

- The extended trace port
- Logic analyzer connection
- Link to Agilent's logic analyzer

Performance issues

- Area and Timing Optimization
- Introduction Plan Ahead

Application examples and exercises