

ExpressWorkshop FPGA Virtex-5

With the availability of virtex-5 family the effective implementation of large complex design is possible. The virtex-5 architecture consist of variety of new features like 6-input LUT, better block ram and FIFO implementation, high speed memory interfaces and advanced DSP applications. The focus of this workshop is to explain the description of modified adorned architectural elements and their optimal implementation with VHDL. In addition to this software support by core generator and Architecture Wizard will be explained.

Applicable technologies

Virtex-5

Requirements

Basic knowledge of digital technology is helpful

Duration and Cost

Duration: 1 day

Cost: € 180, – net per person, including detailed training material, drinks in the breaks and lunch.

Agenda

Introduction Virtex-5 Technology

- Virtex-5 Platforms

Introduction ISE Design-Software

- Project management
- Design Entry
- Synthesis and Verification
- Implementation

Clocking Resources

- Clock Manager Technology
- DCM
- Phase Lock Loops
- Global and regional clock networks
- Application examples

I/O Resources

- SelectIO resource: IOB
- SelectIO logic resources: ILOGIC, OLOGIC, IODELAY, IDELAYCTRL
- SelectIO advanced logic resources : ISERDES, OSERDES
- New I/O standards
Core Resources and Embedded Blocks
- 6-input LUT
- CLB
- Connectivity
- Distributed memories
- RAMB36: Block RAM application examples and Block RAM ECC
- FIFO36 and application examples
- Overview: DSP48E, embedded cores, serial I/O

Configuration Overview