

ExpressWorkshop VHDL

VHDL Programmierung leicht gemacht

Due to the constantly rising demand for great complex logic modules with high clock rates, the challenges for user are also growing steadily. Due to this fact the user forced powerfully at the hardware description language based design methodologies in order to fulfill the demand for the shortest development time and provide greater flexibility for changes and to secure the economic success of company. This workshop gives an overview of the concept of VHDL, and the typical VHDL design cycle. The PLC2 is an authorized design and training center of Xilinx cooperating in Xilinx expert and customer education program and specialized for Xilinx technology since 15 years.

Applicable technologies

All CPLDs / FPGAs

Requirements

None

Duration and Cost

Duration: 1 day

Cost: € 180, – net per person, including detailed training material, drinks in the breaks and lunch.

Agenda

Introduction to VHDL

- Levels of Abstraction
- Language Concept
- HDL Design Flow
- VHDL Simulation
- VHDL Synthesis

Modeling with VHDL

- VHDL Design Units
- Entity
- Architecture

VHDL Operators

- Logical Operators
- Relational Operators
- Arithmetic Operators

Structural Modeling

- Signal Declaration
- Hierarchy
- Component Declaration and Instantiation

Concurrent and Sequential Statements

- Sequential Statements
- Concurrent Statements

Processes

- Process and Process Examples
- Controlling the sequential code