

# ExpressWorkshop FPGA Spartan-3

The Express workshop “Spartan-3” educate the participant in the architecture of Spartan-3 FPGAs. The focus of this workshop is on the basic architectural elements of all Spartan-3 devices and their optimal implementation with VHDL. The overview of development environment ISE will be given and its options will be discussed. The basic command of description language VHDL for synthesis and simulation are not the part of this workshop. The basic knowledge of VHDL can be achieved in PLC2 other workshops like “Professional VHDL” or “Compact VHDL”. In the final section of the workshop an example will be implemented and verified on the real hardware (Xilinx Spartan-3 evaluation board).

## Applicable technologies

Spartan-3 Series

## Requirements

Basic knowledge of VHDL and digital technology are helpful

## Duration and Cost

Duration: 1 day

Cost: € 180, – net per person, including detailed training material, drinks in the breaks and lunch.

## Agenda

### The architecture of the Spartan-3 FPGAs

- IOBs
- CLBs (LUT, SRL16, distributed RAM)
- BlockRAM
- Clocking (IBUFG, DCM, BUFGMUX)
- Carry and Arithmetic Logic

### Introduction to the ISE design software

### Implementation options

- Synthesis
- MAP
- Place & Route

### I/O Resources

- SelectIO resource: IOB
- I/O standards

### Configuration overview

- Configuration mode
- Relevant pins
- Implantation