

ExpressWorkshop FPGAs for DSP

The ExpressWorkshop „FPGA for DSP“ demonstrate the participant wide range of FPGA based DSP Applications. After a basic introduction to the FPGA development, the architecture of FPGA will be discussed from the view-point of designing DSP specific functions such as Multipliers, MAC, and FIR/IIR filter design. Depend upon the required sampling frequency the DSP functions realized in different ways. After discussing the theoretical concepts mentioned above, a practical example will be presented. The seminar participant should have the basic knowledge of hardware description language VHDL and DSP basics are an advantage. To continue further with more detailed

DSP concepts, participant can attend the other DSP workshops offered by PLC2.

Applicable technologies

All kind of FPGA technologies

Requirements

None

Duration and Cost

Duration: 1 day

Cost: € 180, – net per person, including detailed training material, drinks in the breaks and lunch.

Agenda

- Architecture of the Virtex II FPGAs
- CLBS and SLICES
- DCM and Clock Distribution
- Embedded Multiplier
- Distributed RAM and Block RAM
- IOBs and DCI

Implementation of DSP functions

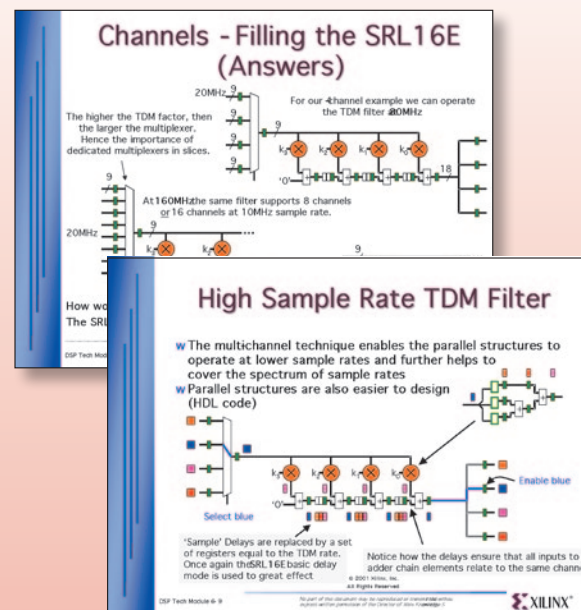
- General design flow
- The VHDL design flow

Optimal use of specific technical DSP functions

Implementation of various DSP Applications

Download the target hardware (Virtex II test board)

Summary, questions and discussion



Channels - Filling the SRL16E (Answers)

The higher the TDM factor, then the larger the multiplexer. Hence the importance of dedicated multiplexers in slices.

For our 4-channel example we can operate the TDM filter @20MHz

At 160MHz the same filter supports 8 channels or 16 channels at 10MHz sample rate.

High Sample Rate TDM Filter

The multichannel technique enables the parallel structures to operate at lower sample rates and further helps to cover the spectrum of sample rates

Parallel structures are also easier to design (HDL code)

Sample Delays are replaced by a set of registers equal to the TDM rate. Once again the SRL16E basic delay mode is used to great effect

Notice how the delays ensure that all inputs to adder chain elements relate to the same channel

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