

## Workshop

# Verification of Reflections and Crosstalk

New technologies allow FPGA interface with high clock rates and data rates, this factor forced the developer to consider the effect of signal integrity. The 1-day workshop on “Verification of Reflection and Crosstalk with HyperLynx” teaches the participant to understand the use of HyperLynx in the analysis of reflection and crosstalk on board. Based on the properties of I/O level programmable logic, it will be shown how the cable length affects the signal integrity. This effect can't be ignored and must be taken in to account. Especially when reflection and crosstalk received. Using HyperLynx It will be demonstrated

how these effects can be modeled and simulated. Various measures to improve signal integrity will be demonstrated.

### Applicable technologies

SPARTAN-3 Families, Virtex-4, Virtex-5

### Requirements

Basic Knowledge of XILINX FPGAs.

### Duration and Cost

Duration: 1 day

Cost: € 600, – net per person, including detailed training material, drinks in the breaks and lunch.

## Agenda

### Transmission Lines

- Basics
- Critical trace length

### Introduction to Hyperlynx

### IBIS Models

- IBIS standard
- IBIS modeling
- IBIS editor

### Verification of Reflections

- Reflection effects and calculation
- Minimizing reflections: trace termination

### Verification of Reflections

- Crosstalk effects and calculations
- Minimizing crosstalk