

PowerWorkshop Professional DSP for XILINX FPGAs

This PowerWorkshop closes the gap between DSP system designers and hardware developers and has a very high practical content. It is designed for FPGA developers who have little or no experience of DSP. After a comprehensive introduction to the architectural features of XILINX FPGAs that are especially important for DSP applications, you will learn how DSP algorithms can be efficiently implemented in FPGAs. You will also be shown how decisions at system level can influence the implementation and function of the DSP application. In the board based practical part you will describe and verify on your own circuits from all kinds of DSP application areas with VHDL. After the concluding synthesis, you will verify the correct functioning of these circuits by porting them onto real systems/test boards.

As well as the test board, each participant will be given all

the necessary equipment such as a development computer with design software, power pack, signal generator and oscilloscope. This gives them the best possible idea of the real and practical job of the developer. Naturally you can also work on concrete assignments as part of the practical section.

Applicable technologies

Spartan3 / Virtex II / Virtex4 FPGAs

Requirements

ISE Design Basics, Fundamentals of VHDL

Duration and Cost

Duration: 5 days

Cost: € 2900, – net per person, including detailed training material, drinks in the breaks and lunch.

Agenda

Basic DSP

- Basic terminology and acronyms used in DSP design
- Sample rates and bit widths used in DSP applications
- DSP Building blocks and processing requirements

Representing numbers

- Numbering formats, range and precision
- Mathematical operations using a variety of formats

FPGA DSP resources

- Structure and resources of XILINX devices
- Estimating DSP building block sizes & Implementing the multiplication function

Bit width impact on system level decisions

- On Chip Memory
- Block versus Distributed memory & Memory aspect ratios and their manipulation
- SRL16E and the delay function

Designing Filters

- FIR filter specifications and implementations & Selection of a technique for a given specification
- Effects of half band and interpolated filters
- Creating an SDA FIR filter with Core Generator

Designing DSP Systems

- Rate changing and how it effects FIR filter choice
- Filtering algorithms that exploit device architecture
- Importance of connectivity versus isolated functions

Overview FFT Design

- Strategies for FFT implementation & Achieving bandwidth requirements of the FFT

Verification of DSP Designs

- Test Benches incl. external components
- Modelling external components (ADC, Amplifier, DAC)

Labs