

Workshop

Designing with PCI Express

PCI Express is becoming more and more important. With the availability of a soft core, new fields of application are opening up for FPGAs, and the design and system application of PCI Express requires comprehensive know-how. The 3-day PLC2 workshop “Designing a PCI Express System” trains FPGA designers in the effective application of this LogiCore, thus enabling them to implement the requirements from the PCI Express specification with the XILINX PCI Express LogiCore solution. As well as the basics of the protocol, this workshop covers the possible applications of the PCI Express LogiCore, allowing the developer to produce their design more quickly and effectively. The workshop is aimed at FPGA designers who want to implement PCI Express with SPARTAN-

3/-3E/-3A, VirtexII-Pro or Virtex-4 technologies. If no MGTs are available, the serial link can be implemented with an external PCI Express SERDES.

Applicable technologies

Virtex-5 (also Spartan-3 / Virtex-4)

Requirements

Basic VHDL
Basic ISE and ModelSim

Duration and Cost

Duration: 3 day

Cost: € 1850, – net per person, including detailed training material, drinks in the breaks and lunch.

Agenda

Introduction Virtex-5 Technology

PCIe Layers

- Architecture
- Packet Routing
- Packet Assembly / Disassembly
- Packet Types and Transfers

PCIe Protocol

- Transaction Types
- TLP Fields
- TLP Requests

PCIe Configuration Space

- Legacy and PCIe Configuration

XILINX PCIe Endpoint Cores

- Embedded Core
- Softcores
- PCIe and CoreGen
- Local Link Interface
- Native Interface
- Control Interfaces
- Errors and Interrupts

PCIe Board Design Considerations

- Clocking
- Physical Layer Topics
- PCIe Debugging
- Mechanicals, Hot Plug, Power
- Board Design Issues

PCIe Endpoint Application Example

- Basics
- DMA Transfer
- Application Example

Labs

- Constructing the Endpoint Core
- Simulating the Design
- Implementing the Design
- Running Diagnostics
- Running Application