

Workshop

Designing a PCI-X System with XILINX FPGAs

The availability of cutting-edge programmable technologies with high complexities, combined with complex parameterizable IP core cells is opening up new possibilities for system developers. The new standard PCI-X is a downward-compatible extension of the familiar PCI standard and offers the user an up to eight-fold transmission bandwidth based on the PCI standard. The LogiCore PCI-X core cell is a completely verified PCI-X function macro with guaranteed function and timing behavior. This allows complex PCI-based systems to be developed and verified in the shortest time. The official XILINX Design and Training Center PLC2 is a collaborator on the XILINX Xperts and XILINX Customer Education Program and has been specializing in XILINX technologies for more than 15 years. The 3-day PLC2 workshop “Designing a PCI-X System with XILINX FPGAs” provides an overview of the basics of the PCI-X standard and concentrates

on the development of initiator/target applications using the LogiCore PCI-X cell. You will learn to define, verify and develop your own PCI-X based systems, and the theoretical content will be rounded off with exercises on the PC.

Applicable technologies

All XILINX FPGA technologies available for the PCI core cells

Requirements

Detailed knowledge of the ISE design system Fundamentals VHDL

Duration and Cost

Duration: 3 days

Cost: € 1800, – net per person, including detailed training material, drinks in the breaks and lunch.

Agenda

PCI-X Fundamentals

- Differences between PCI and PCI-X
- Local Bus Architecture
- Signals and Terminology
- Protocol Rules
- 64-Bit Transactions
- Device Specification

XILINX PCI-X Solutions

- Introducing the XILINX LogiCore PCI-X Interface
- Overview of XILINX PCI-X LogiCore Operation

- The User Configuration Module
- How the LogiCore represents PCI-X bus signals
- How the User-Application Interface works

Designing with the XILINX PCI-X Interface

- Interfacing buffers with the PCI-X LogiCore
- Designing a Target engine
- Designing an Initiator engine
- Handling Configuration Transactions
- Handling PCI transactions

Exercises on PC