

## Workshop

# Designing with Virtex-5 Multi-Gigabit Serial I/O

The new Virtex-5 LXT, SXT and FTX families allow serial interfaces in the Gbit/s range. This involves the use of new transceivers, which require comprehensive know-how for quick and effective use. The 3-day PLC2 workshop “Designing with Virtex-5 Multi-Gigabit Serial I/O” is aimed at developers who want to implement serial interfaces in the Gbit/s range and use them in a system. This workshop enables developers to effectively use all available features of the RocketI/Os, define the interfaces and attributes necessary for the features, and instantiate the RocketI/O primitives with the Architecture Wizard integrated in the CoreGenerator, in order to implement project-specific interfaces or standardized serial interfaces. The Serial I/O Toolkit for ChipScope is used to show

an effective verification of the serial transmission link. Signal-integrity topics, including a simulation example and pointers on board design, provide practical tips for implementation.

### Applicable technologies

Virtex-5 LXT/SXT/FTX

### Requirements

Basic knowledge of VHDL and FPGA Implementation

### Duration and Cost

Duration: 3 day

Cost: € 1850, – net per person, including detailed training material, drinks in the breaks and lunch.

## Agenda

### Introduction

- Virtex-5 technology overview
- Virtex-5 clocking resources

### Clocking, timing and RESET

### Physical Coding Sublayer

- Fabric interface
- Encoding / decoding
- Symbol alignment
- Clock correction
- Channel bonding
- CRC

### Implementation and Verification

- RocketIO Wizards
- Example Design
- Smart model simulation
- ChipScope IBERT tool

### Physical Media Attachment

- Serial I/O
- Pre-Emphasis and equalization

### Board Design Considerations

- Powering RocketIOs
- Bypassing
- Routability and trace geometries
- Board level link simulation

### Application Examples

- Gigabit Ethernet
- SDH/SONET
- Aurora

### Labs

- Coding/encoding lab
- Using Commas and K-character symbols
- CRC feature
- Clock correction
- Channel bonding
- Implementation example
- Link verification using ChipScope Serial I/O Tool Kit