

Workshop DSP Implementation Techniques for XILINX FPGAs

The workshop “DSP Implementation Techniques for XILINX FPGAs” closes the gap between DSP system designers and hardware developers. As well as explaining how DSP algorithms can be efficiently implemented, it also shows how decisions at system level can influence both the development process and the product costs. This workshop is thus aimed at developers who are familiar with product developments requiring digital signal processing. It focuses on system design, hardware design and DSP algorithms. Although the workshop begins with a brief outline of the basic DSP theory, you should have a fundamental knowledge of the following areas:

- Scanning frequencies and FIR (Finite Impulse Response) and IIR (Infinite Impulse Response) filter

- Oscillators, mixers and FFT (Fast Fourier Transformation) algorithms.

The theoretical content will be rounded off with exercises on the laptop/PC.

Applicable technologies

Spartan3 / Virtex2 / Virtex4 FPGAs

Requirements

ISE Design Basics, Fundamentals of VHDL

Duration and Cost

Duration: 3 days

Cost: € 1850, – net per person, including detailed training material, drinks in the breaks and lunch.

Agenda

„Being on the same wavelength“

- Basic terminology and acronyms used in DSP design
- Sample rates and bit widths used in DSP applications
- DSP Building blocks and processing requirements

„Some Bits about Numbers“

- Numbering formats, range and precision
- Mathematical operations using a variety of formats

„Tuning the receiver“

- Structure and resources of XILINX devices
- Estimating DSP building block sizes & Implementing the multiplication function
- Bit width impact on system level decisions

„Memories are Made of This“

- Block versus Distributed memory & Memory aspect ratios and their manipulation
- SRL16E and the delay function

„Selective Filters“

- FIR filter specifications and implementations & Selection of a technique for a given specification
- Effects of halfband and interpolated filters
- Creating an SDA FIR filter with Core Generator

„One Filter Doesn't Make a System“

- Rate changing and how it effects FIR filter choice
- Filtering algorithms that exploit device architecture
- Importance of connectivity versus isolated functions

„Dont Block the Data Path“

- Strategies for FFT implementation and Achieving bandwidth requirements of the FFT

Exercises on PC